Attorney's Docket No.:10559-350001/P10068

REMARKS

Reconsideration and allowance of the above-referenced application are respectfully requested.

Claims 22 has been amended to provide proper antecedent for the system crash. Claim 41 has also been amended to enjoy proper antecedent.

Initially, claims 13 and 16-21 were canceled in error in the last amendment. These claims have been re-added herein as new claims 48-54 respectively. Applicants apologize for this error.

Claims 1-4, 9, 12, 33, 35 and 46 stand rejected under 35 USC 102 as allegedly being anticipated by Coteus et al. contention is respectfully traversed.

As previously discussed, claim 1 defines that the arbitration logic includes a first element "which produces a set of first values for said register ... and ... dithers between different sets of values and determines which of said plurality of values produces a best desired result". The rejection alleges that this is shown in Coteus et al. page 10 of the rejection alleges that figures 3E and 3F show determining different values. However, these different values are stored as 16Al and 16A2, but the arbitration logic does not store sets of values, tests those sets of values, and use the set that

Attorney's Docket No.: 10559-350001/P10068

produces the best result. Rather, the arbitration logic, as clearly shown in figures 3E and 3F calculates certain values, see steps x2 and x3; and then determines averages of values, and sets the delay based on these calculations - not based on selecting a set. Calculating values is very different then the claimed checking different sets of values.

Claim 1 requires, for example, that the arbitration logic "dithers between different sets of values and determines which of said plurality of values produces a best desired result". This is very different than calculating values, and choosing the best calculated value. In contrast to the system of Coteus et al which calculates the value, claim 1 requires choosing which of a plurality of sets produces the best result. There is no teaching or suggestion in Coteus et al of storing multiple sets of values, as claimed, and testing each of the sets. Therefore, claim 1 should be allowable, along with claims 2-4, 9 and 12 which depend therefrom.

Claim 33 similarly requires providing "sets of values...". Claim 33 also requires testing the signals to determine relative amounts and finding the best one of the sets. Nothing in Coteus et al teaches or suggests testing sets of values, as claimed and selecting one, as claimed.

Claim 22 was rejected over Coteus et al in view of the Upgrading and Repairing reference which is newly cited. Coteus Attorney's Docket No.:10559-350001/P10068

et al teaches nothing about storing new delay values in response to detecting a system crash as apparently acknowledged at page 5, paragraph B of the official action. Coteus et al does teach that the method is started when the system is powered on, see column 10, lines 20-26, and column 24, lines 66-column 25, line 5. Note however, that column 25 beginning at lines 65 of Coteus et al teaches that the information, obtained at power up "may be stored permanently in the memory 3" see column 26, lines 2-3. Therefore, it is clear that the teaching of Coteus et al is not that signals be re-obtained at every power up, but rather that the signals be permanently stored.

The secondary reference entitled Upgrading and Repairing PC's clearly does teach a power on self test, but teaches nothing about re-storing delay values of this type, responsive to a crash. A simple teaching of power on self test teaches nothing about storing new delay values responsive to a system crash. Moreover, as described above, Coteus et al actually teaches away from storing new delay values during a crash: Coteus et al rather teaches that delay values are stored once and then maintained.

Therefore, claim 22, as well as the claims which depend therefrom, should be allowable for these reasons.

Claim 37 defines using the values to cause signal delays when a system crash is not detected. Only when a system crash Attorney's Cocket No.:10559-350001/P10068

is detected, claim 37 requires determining new delays and causing new signal delays based on those delay values. As described above, this goes entirely against the teaching of Coteus et al in view of Upgrading and Repair. Therefore, these claims should be allowable for these reasons.

In view of the above amendments and remarks, therefore, all of the claims should be in condition for allowance. A formal notice to that effect is respectfully solicited

It is believed that all of the pending claims have been addressed in this paper. However, failure to address a specific rejection, issue or comment, does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above are not intended to be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

Attorney's Docket No.:10559-350001/P10068

Applicant asks that all claims be allowed. Please apply any charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: November 19, 2004

Soott C. Harris

Attorney for Intel Corporation

Reg. No. 32,030

Fish & Richardson P.C.

PTO Customer Number:

20985

12390 El Camino Real San Diego, CA 92130

Telephone: (858) 678-5070 Facsimile: (858) 678-5099

10458693.doc